**Processor Design Project**

**Interim Report**

**EE480**

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# Introduction

# Instruction Set Architecture Development

The instruction set architecture defines the computer architecture and capabilities by detailing the data types, possible instructions, registers, memory addressing modes, interrupt control, and data input/output control. Defining the instruction set architecture enables programming the computer architecture, assembly instructions and associated parameters are translated to machine code.

## Implementation

This accumulator computer architecture includes 16 opcodes with multiple flags, which describe addressing modes and specific opcode operation. Each instruction is implemented as 16-bits wide (one word) for this accumulator processor, which features an 8-bit data bus. 4-bits are reserved for the opcode, 2-bits are reserved for the opcode flag, and 10-bits are allocated for the operand. Table 1 provides an overview of the instruction structure. The size of the operand is 10-bits; however the legal size of operands is limited by the size of the data bus, 8-bits wide.

Table - Instruction Structure

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | 15:12 | 11:10 | 9:0 |
| Field | OPCODE | FLAG | OPERAND |

Each of the 16 opcodes are detailed in the following sections by OPCode, flags, assembly format, machine code format, description of operation, architecture level operation, and memory addressing.

### Add

|  |  |
| --- | --- |
| Instruction | Add |
| OPCode | 0000 |
| Flags | 00: Direct 01: Indirect 10: Immediate |
| Format | ADD FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 0000 | xx | RAM ADDR / INTEGER | |
| Description | Adds the specified operand to the current contents of the ACC register. The Output from the ALU will be returned to the ACC register. |
| Operation | ACC ← ACC + OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Sub

|  |  |
| --- | --- |
| Instruction | SUB |
| OPCode | 0001 |
| Flags | 00: Direct 01: Indirect 10: Immediate |
| Format | SUB FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 0001 | xx | RAM ADDR / INTEGER | |
| Description | Subtracts the specified operand from the current contents of the ACC register. The Output from the ALU will be returned to the ACC register. |
| Operation | ACC ← ACC - OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Logical OR

|  |  |
| --- | --- |
| Instruction | OR |
| OPCode | 0011 |
| Flags | 00: Direct 01: Indirect 10: Immediate |
| Format | OR FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 0011 | xx | RAM ADDR / INTEGER | |
| Description | Perform a LOGICAL OR operation of contents in Accumulator and OPERAND. The result of the operation will be stored in the accumulator. |
| Operation | ACC ← ACC | OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Logical AND

|  |  |
| --- | --- |
| Instruction | AND |
| OPCode | 0100 |
| Flags | 00: Direct 01: Indirect 10: Immediate |
| Format | AND FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 0100 | xx | RAM ADDR / INTEGER | |
| Description | Perform a LOGICAL AND operation of contents in Accumulator and OPERAND. The result of the operation will be stored in the accumulator. |
| Operation | ACC ← ACC & OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Logical Complement (COMP)

|  |  |
| --- | --- |
| Instruction | COMP |
| OPCode | 1111 |
| Flags | 00 |
| Format | COMP FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 1111 | 00 | 0000000000 | |
| Description | Perform LOGICAL complement/Negation on the contents of the accumulator register. The complement will be stored in the accumulator register. |
| Operation | ACC ← NOT ACC |
| Memory Addressing | N/A |

### Multiply and Divide

|  |  |
| --- | --- |
| Instruction | MUL |
| OPCode | 0010 |
| Flags | 00: Direct 01: Indirect |
| Format | MUL FLAG OPERAND [Lower 4 bits] |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 0010 | 00 01 | RAM ADDR | |
| Description | Performs multiplication on lower 4-bits of Accumulator and lower 4-bits of the operand. |
| Operation | ACC ← ACC \* OPERAND |
| Memory Addressing | Direct and Indirect |

|  |  |
| --- | --- |
| Instruction | DIV |
| OPCode | 0010 |
| Flags | 10: Direct 11: Indirect |
| Format | DIV FLAG OPERAND [Lower 4 bits] |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 0010 | 10 11 | RAM ADDR | |
| Description | Performs division on lower 4-bits of Accumulator and lower 4-bits of the operand. |
| Operation | ACC ← ACC / OPERAND |
| Memory Addressing | Direct and Indirect |

### Arithmetic Left/Right Shift

|  |  |
| --- | --- |
| Instruction | SHFT |
| OPCode | 0101 |
| Flags | 00: Left Shift in 0 01: Left Shift in 1 |
| Format | SHFT FLAG OPPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 0101 | 00 01 | INTEGER < 7 | |
| Description | Performs a LEFT SHIFT operation on the contents of the accumulator register. The value of the bit shifted in is dependent upon the provided flag. Any number of bits less than 7. |
| Operation | ACC ← ACC [N-2:0 + (FLAG BIT)\*OPERAND] |
| Memory Addressing | N/A |

|  |  |
| --- | --- |
| Instruction | SHFT |
| OPCode | 0101 |
| Flags | 10: Right Shift in 0 11: Right Shift in 1 |
| Format | SHFT FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 0101 | 10 11 | INTEGER < 7 | |
| Description | Performs a RIGHT SHIFT operation on the contents of the accumulator register. The value of the bit shifted in is dependent upon the provided flag. Shift by any number of bits less than 7. |
| Operation | ACC ← ACC [OPERAND\*(FLAG BIT) + N-1:1] |
| Memory Addressing | N/A |

### Conditional Branch

|  |  |
| --- | --- |
| Instruction | BRA |
| OPCode | 0110 |
| Flags | 00: Branch if equal 01: Branch Less Than 10: Branch Greater Than |
| Format | BRA FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 0110 | 10 11 10 | MEM ADDR | |
| Description | Performs a comparison between the Accumulator and Operand. If true, jump to instruction pointed to by OPERAND. |
| Operation | IP ←IP + OPERAND |
| Memory Addressing | N/A |

### Unconditional Jump

|  |  |
| --- | --- |
| Instruction | JMP |
| OPCode | 0111 |
| Flags | NULL |
| Format | JUMP OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 0111 | 00 | MEM ADDR | |
| Description | Executes an unconditional branch. When encountered the instruction pointer is adjusted to the operand target memory address. |
| Operation | IP ←IP + OPERAND |
| Memory Addressing | N/A |

### Jump/Return to/from a Subroutine

|  |  |
| --- | --- |
| Instruction | RTS |
| OPCode | 1000 |
| Flags | NULL |
| Format | RTS |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 1000 | 00 | 0000000000 | |
| Description | Transfer program control to the address located in the implied return address. Return is made to the top element in the PC stack. Should also pop the ACC value from the ACC stack. |
| Operation | PC ← Implied Address (From Stack) |
| Memory Addressing | NULL |

### Return from Interrupt Service Routine

|  |  |
| --- | --- |
| Instruction | RTI |
| OPCode | 1001 |
| Flags | NULL |
| Format | RTI |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 1001 | 00 | 0000000000 | |
| Description | Return from an Interrupt Subroutine to the position the PC was at before the interrupt. The PC location to return to will be the top element in the PC stack. |
| Operation | PC ← Return Address (From Stack) |
| Memory Addressing | NULL |

### LOAD Accumulator

|  |  |
| --- | --- |
| Instruction | LOAD |
| OPCode | 1010 |
| Flags | 00: Direct 01: Indirect  10: Immediate |
| Format | LOAD FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 1010 | 00 01 10 | MEM ADDR MEM ADDR Integer | |
| Description | **Direct Mode** Copy the contents of the address in RAM specified by the source operand to the accumulator.  **Indirect Mode:** Copy the accumulator to the destination memory address found at the memory address of the operand  **Immediate Mode:** Copy the 8-bit immediate source operand to the accumulator. |
| Operation | **Direct Mode** ACC ← memory (OPERAND)  **Indirect Mode:**  ACC ← Memory{ memory( OPERAND) }   **Immediate Mode:** ACC ← IMMED OPERAND |
| Memory Addressing | Direct, Immediate |

### STORE Accumulator to RAM

|  |  |
| --- | --- |
| Instruction | STORE |
| OPCode | 1011 |
| Flags | 00: Direct 01: Indirect |
| Format | STORE FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 1011 | 00 01 | MEM ADDR | |
| Description | **Direct Mode** Copy the accumulator to the destination memory address specified by the operand **Indirect Mode:** Copy the accumulator to the destination memory address found at the memory address of the operand |
| Operation | **Direct Mode** memory(OPERAND) ← ACC **Indirect Mode:** Memory{ memory( OPERAND) } ← ACC |
| Memory Addressing | Direct, Indirect |

### INPUT Data Word to RAM

|  |  |
| --- | --- |
| Instruction | INPUT |
| OPCode | 1100 |
| Flags | 00: Direct 01: Indirect |
| Format | INPUT FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 1100 | 00 01 | MEM ADDR | |
| Description | Input a data word to RAM |
| Operation | **Direct Mode** memory(OPERAND) ← I/O Port  **Indirect Mode:** Memory{ memory( OPERAND) } ← I/O Port |
| Memory Addressing | Direct, Indirect |

### OUTPUT Data Word from RAM

|  |  |
| --- | --- |
| Instruction | OUTPUT |
| OPCode | 1101 |
| Flags | 00: Direct 01: Indirect |
| Format | OUTPUT FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 1101 | 00 01 | MEM ADDR | |
| Description | Output data word from RAM |
| Operation | **Direct Mode** memory(OPERAND) → I/O Port  **Indirect Mode:** Memory{ memory( OPERAND) } → I/O Port |
| Memory Addressing | Direct, Indirect |

### LOAD Mask Register of HVPI

|  |  |
| --- | --- |
| Instruction | LOAD Mask Register of HVPI |
| OPCode | 1110 |
| Flags |  |
| Format |  |
| Description |  |
| Operation |  |
| Memory Addressing |  |

### NOP

|  |  |
| --- | --- |
| Instruction | NOP |
| OPCode | 1111 |
| Flags | 11 |
| Format | NOP |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:12 | 11:10 | 9:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 1111 | 11 | 0000000000 | |
| Description | Performs no operation. |
| Operation | NULL |
| Memory Addressing | NULL |

# Accumulator Architecture Development

## Architecture Overview



Figure - Top Level Architecture Overview

## Instruction Implementation

### Add

### Sub

### Logical OR

### Logical AND

### Logical Complement (COMP)

### Multiply and Divide

### Arithmetic Left/Right Shift

### Conditional Branch

### Unconditional Jump

### Jump/Return to/from a Subroutine

### LOAD Accumulator from RAM

### STORE Accumulator to RAM

### INPUT Data Word to RAM

### OUTPUT Data Word from RAM

### LOAD Mask Register of HVPI

### NOP

## Direct Mapped Cache



Figure - Direct Mapped Cache Flow Diagram

# Conclusion

# References